AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) An apparatus, comprising:

a comparator to receive an analog input signal V_{IN} along with a comparison signal V_C and to generate a digital result , the comparison signal V_C being received at a comparison node ; ~~and~~

~~an adjustment circuit to adjust the comparison signal based on successive digital results from the comparator~~

a higher-threshold sample and hold element to receive V_C and to selectively provide V_H to a higher-threshold node;

a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node;

a lower-threshold sample and hold element to receive V_C and to selectively provide V_L to a lower-threshold node; and

a lower-threshold resistor coupled between the lower-threshold node and the comparison node .

2. (currently amended) The apparatus of claim 1, wherein ~~the adjustment circuit includes:~~

~~an higher-threshold portion associated with a higher-threshold signal V_H; and~~

~~a lower-threshold portion associated with a lower-threshold signal V_L; wherein~~ the comparison signal is adjusted based on successive digital results from the comparator and V_C substantially equals $(V_H + V_L)/2$.

3. (currently amended) The apparatus of claim [[2]] 1 , wherein the ~~comparator receives V_e from a comparison node and:~~

~~the higher-threshold portion of the adjustment circuit includes:~~

~~a higher-threshold sample and hold element to receive V_ϵ and to selectively provide V_H to an higher-threshold node, and~~

~~a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node; and~~

~~the lower-threshold portion of the adjustment circuit includes:~~

~~a lower-threshold sample and hold element to receive V_ϵ and to selectively provide V_L to a lower-threshold node, and~~

~~a~~ lower-threshold resistor ~~having~~ has a resistance substantially equal to R ~~and being coupled between the lower-threshold node and the comparison node~~ .

4. (currently amended) The apparatus of claim [[3]] 1 , wherein the higher-threshold and lower-threshold sample and hold elements are amplifiers each having an output that is isolated from an input.

5. (currently amended) The apparatus of claim [[3]] 1 , further comprising:

a first switch coupled between the higher-threshold node and a reference voltage; and

a second switch coupled between the lower-threshold node and ground.

6. (original) The apparatus of claim 5, wherein the first and second switches are to be closed to initialize V_H to the reference voltage and V_L to ground.

7. (original) The apparatus of claim 5, further comprising:

a third switch coupled between the output of the higher-threshold sample and hold element and the higher-threshold node; and

a fourth switch coupled between the output of the lower-threshold sample and hold element and the lower-threshold node.

8. (original) The apparatus of claim 1, further comprising:

a multi-bit result register to store results from the comparator.

9. (currently amended) The apparatus of claim 1, wherein the ~~adjustment circuit~~ apparatus is further to convert multiple digital input signals into an analog output signal V_{OUT}.

10. (currently amended) A method, comprising:

initially setting a higher-threshold signal V_H;

comparing an analog input signal V_{IN} to a comparison signal V_C;

providing a digital result of the comparison;

~~adjusting V_C based on the digital result~~

when a digital result indicates V_{IN} is less than the existing V_C, transferring the existing V_C through a sample and hold element to set V_H to the existing V_C ; and

successively performing comparisons [[, stores,]] and ~~adjustments~~ transfers to generate a digital representation of V_{IN}.

11. (currently amended) The method of claim 10, ~~wherein said adjusting includes~~ further comprising :

~~initially setting a higher-threshold signal V_H; and~~

initially setting a lower-threshold signal V_L, wherein V_C substantially equals $(V_H + V_L)/2$.

12-13. (canceled)

14. (original) The method of claim 11, further comprising:

when a digital result indicates V_{IN} is not less than the existing V_C, setting V_L to the existing V_C.

15. (original) The method of claim 15, wherein V_L is set to the existing V_C by transferring the existing V_C through a sample and hold element.

16. (original) The method of claim 11, wherein V_H is initially set to a reference voltage and V_L is initially set to ground.

17. (original) The method of claim 10, wherein said providing comprising:

storing results in a multi-bit result register.

18. (currently amended) A system, comprising:

a processor having an analog to digital conversion portion that includes:

a comparator to receive an analog input signal V_I along with a comparison signal V_C and to generate a digital result, the comparison signal V_C being received at a comparison node , ~~and~~

~~an adjustment circuit to adjust the comparison signal based on successive digital results from the comparator~~

a higher-threshold sample and hold element to receive V_C and to selectively provide V_H to a higher-threshold node,

a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node,

a lower-threshold sample and hold element to receive V_C and to selectively provide V_L to a lower-threshold node, and

a lower-threshold resistor coupled between the lower-threshold node and the comparison node ; and

a battery input to receive power to be provided to the processor.

19. (currently amended) The system of claim 18, wherein ~~the adjustment circuit includes: an higher-threshold portion associated with a higher-threshold signal V_H; and a lower-threshold portion associated with a lower-threshold signal V_L, wherein~~ the comparison signal is adjusted based on successive digital results from the comparator and V_C substantially equals $(V_H + V_L)/2$.

20. (currently amended) The system of claim 19, wherein the ~~comparator receives V_ϵ from a comparison node and:~~

~~the higher-threshold portion of the adjustment circuit includes:~~

~~a higher-threshold sample and hold element to receive V_ϵ and to selectively provide V_H to an higher-threshold node, and~~

~~a higher-threshold resistor having a resistance R coupled between the higher-threshold node and the comparison node; and~~

~~the lower-threshold portion of the adjustment circuit includes:~~

~~a lower-threshold sample and hold element to receive V_ϵ and to selectively provide V_L to a lower-threshold node, and~~

~~a~~ lower-threshold resistor ~~having~~ has a resistance substantially equal to R ~~and being coupled between the lower-threshold node and the comparison node~~ .